In the Specification:

On page 11, please amend the paragraph beginning at line 14 as follows:

--It may be possible, according to embodiments, to define, which memory area each state machine 20 may access. In case of single mode, it is not required to define different memory areas within memory array 18, as only one set of ports may access memory ~~are~~array 18.--

On page 11, please amend the paragraph beginning at line 20 as follows:

--Figure 3 depicts control port 12, address port 14, and data port 16. Depicted are control port 12, address port 14, and data port 16 divided into two terminals 12a, 14a, 16a, and 12b, 14b, 16b. These two terminals 12a, 14a, 16a, and 12b, 14b, 16b may provide access to memory array 18 by two different processors 8, 10. Each of the port 12, 14, 16 has connection pins. The number of connection pins may determine the bandwidth of the respective bus. ~~A~~As seen in Figure 1, a control bus 11b may be connected to control port 12, an address bus 11a, may be connected to address port 14, and a data bus 11c may be connected to data port 16. The bandwidth of the respective buses may be 8, 16, 32, 64bit, according to embodiments.--